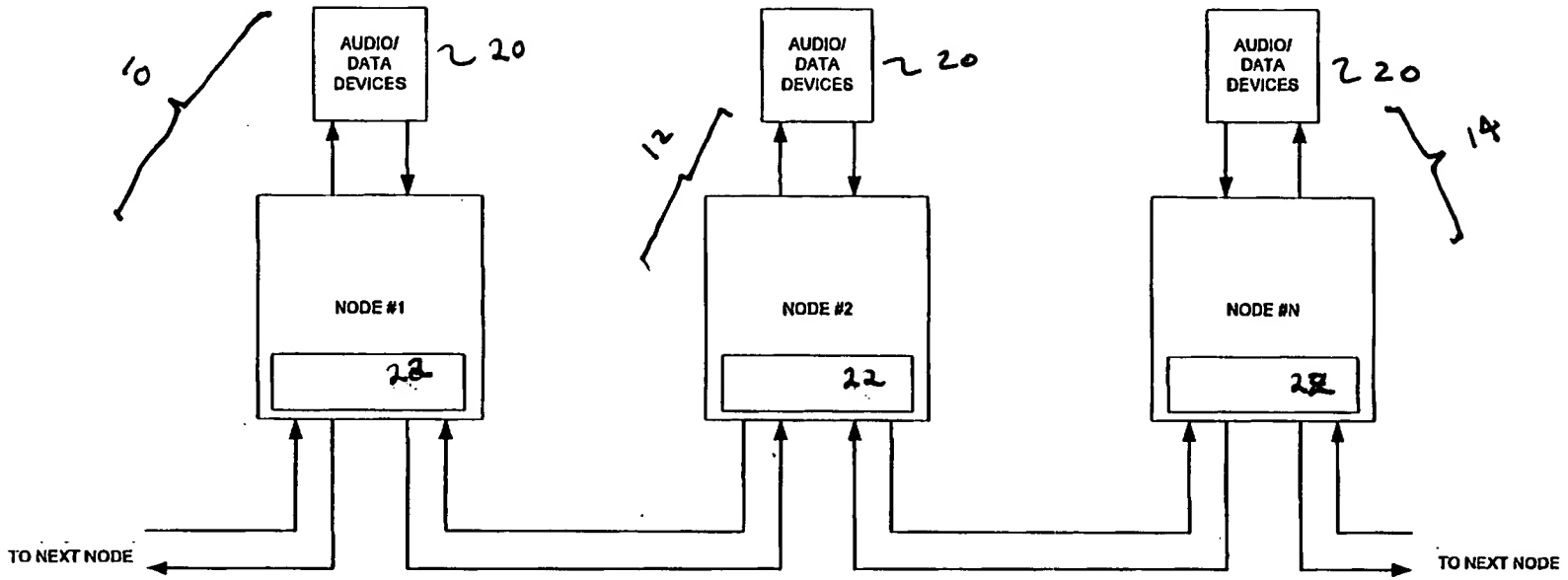


FIG. 1

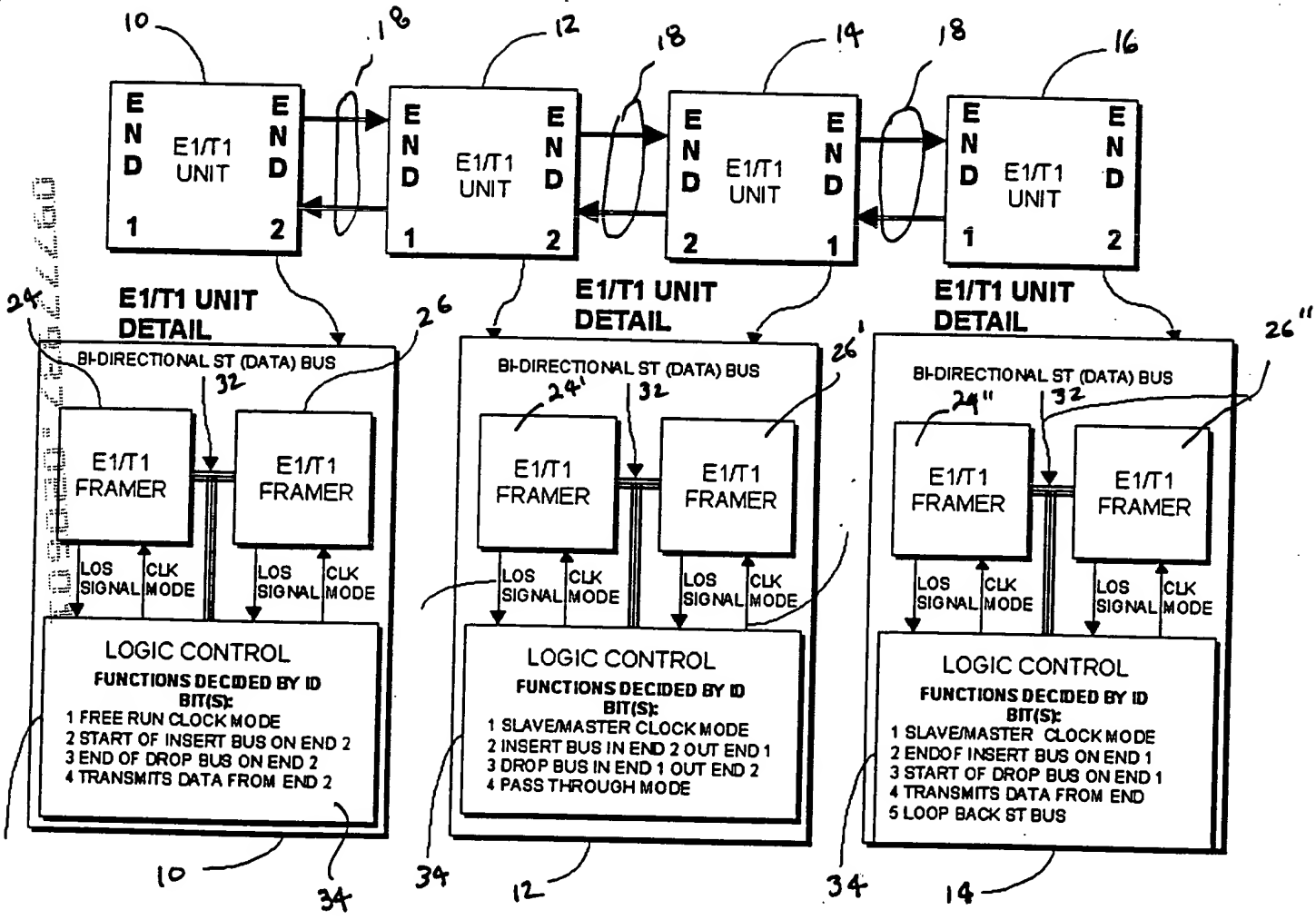
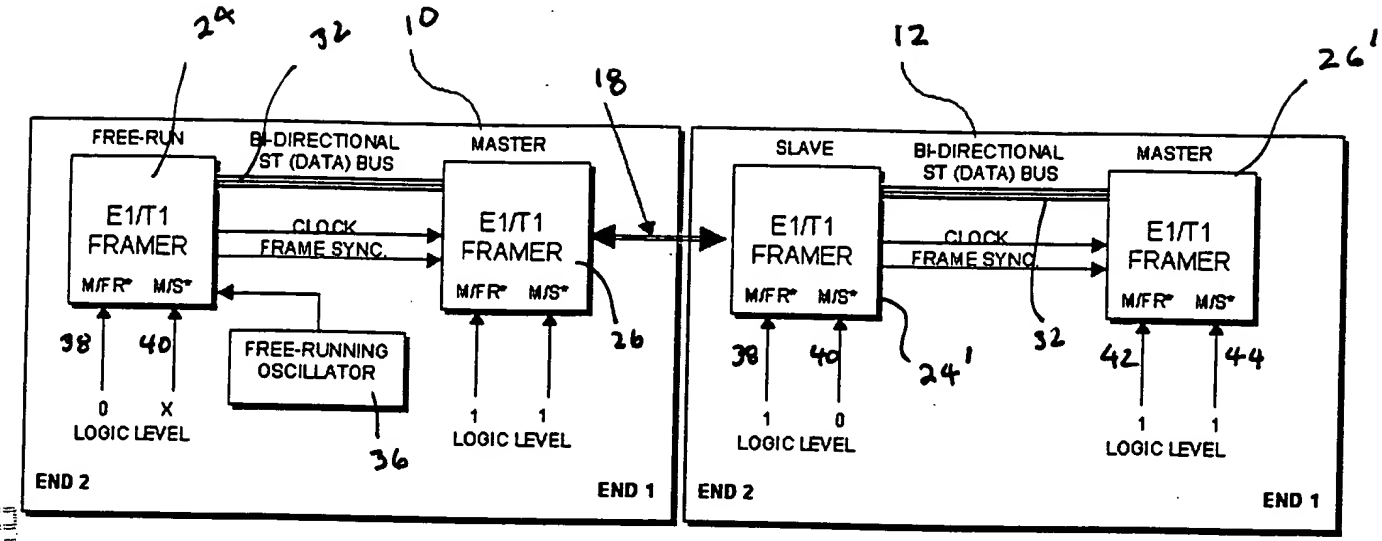

10
18
12
18
14
18
16
END 1
E1/T1 UNIT
END 2
E1/T1 UNIT DETAIL
BI-DIRECTIONAL ST (DATA) BUS
32
E1/T1 FRAMER
LOS SIGNAL
CLK MODE
LOGIC CONTROL
FUNCTIONS DECIDED BY ID BIT(S):
1 FREE RUN CLOCK MODE
2 START OF INSERT BUS ON END 2
3 END OF DROP BUS ON END 2
4 TRANSMITS DATA FROM END 2
1 SLAVE/MASTER CLOCK MODE
2 INSERT BUS IN END 2 OUT END 1
3 DROP BUS IN END 1 OUT END 2
4 PASS THROUGH MODE
1 SLAVE/MASTER CLOCK MODE
2 ENDOF INSERT BUS ON END 1
3 START OF DROP BUS ON END 1
4 TRANSMITS DATA FROM END
5 LOOP BACK ST BUS
24
26
34
12
14

Fig. 2

FIG 3



FRAMER CHIP MODE CONTROL TABLE

INPUT SIGNAL PIN NAME	FREE RUN	SLAVE	FREE RUN	MASTER	MODE
MASTER-SLAVE/NOT FREE RUN	0	1	0	1	
MASTER-NOT SLAVE	X	0	X	1	
	LOGIC LEVEL				

Fig. 3A

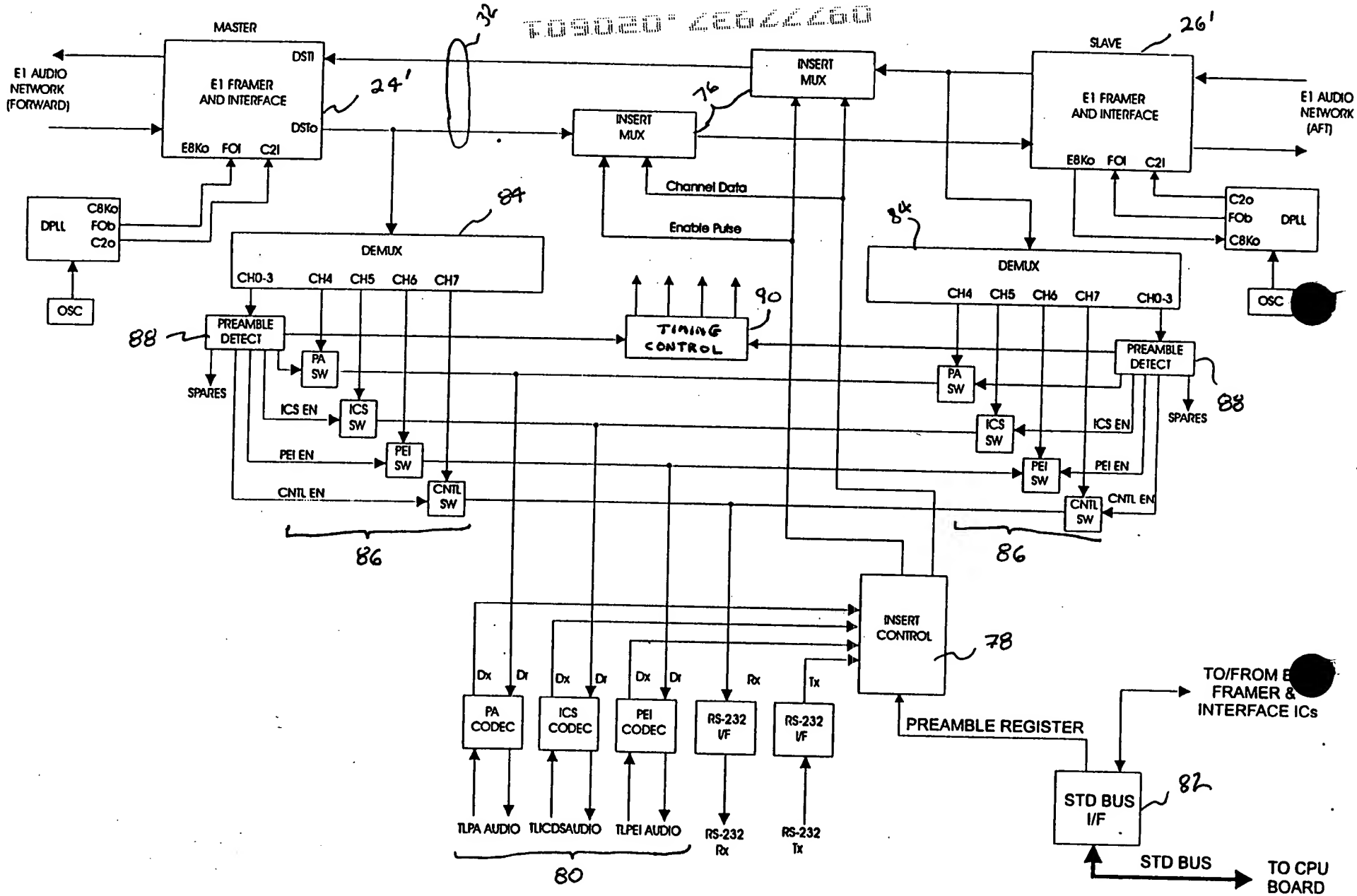

MASTER
E1 AUDIO NETWORK (FORWARD)
E1 FRAMER AND INTERFACE
DSTi
DSTo
E8Ko FOI C2I
24'
32
INSERT MUX
76
INSERT MUX
SLAVE
26'
E1 FRAMER AND INTERFACE
E1 AUDIO NETWORK (AFT)
E8Ko FOI C2I
C2o FOb DPLL C8Ko
DPLL C8Ko FOb C2o
OSC
Channel Data
Enable Pulse
84
DEMUX
CH0-3 CH4 CH5 CH6 CH7
82
DEMUX
CH4 CH5 CH6 CH7 CH0-3
OSC
90
TIMING CONTROL
88
PREAMBLE DETECT
PA SW
SPARES
ICS EN
ICS SW
PEI EN
PEI SW
CNTL EN
CNTL SW
86
PREAMBLE DETECT
PA SW
ICS SW
ICS EN
SPARES
88
PEI SW
PEI EN
CNTL SW
CNTL EN
86
INSERT CONTROL
78
Dx Dr
Dx Dr
Dx Dr
Rx
Tx
PA CODEC
ICS CODEC
PEI CODEC
RS-232 I/F
RS-232 I/F
PREAMBLE REGISTER
TO/FROM E FRAMER & INTERFACE ICs
STD BUS I/F
82
TLPA AUDIO
TLICDSAUDIO
TLPEI AUDIO
RS-232 Rx
RS-232 Tx
80
STD BUS
TO CPU BOARD

FIG. 4

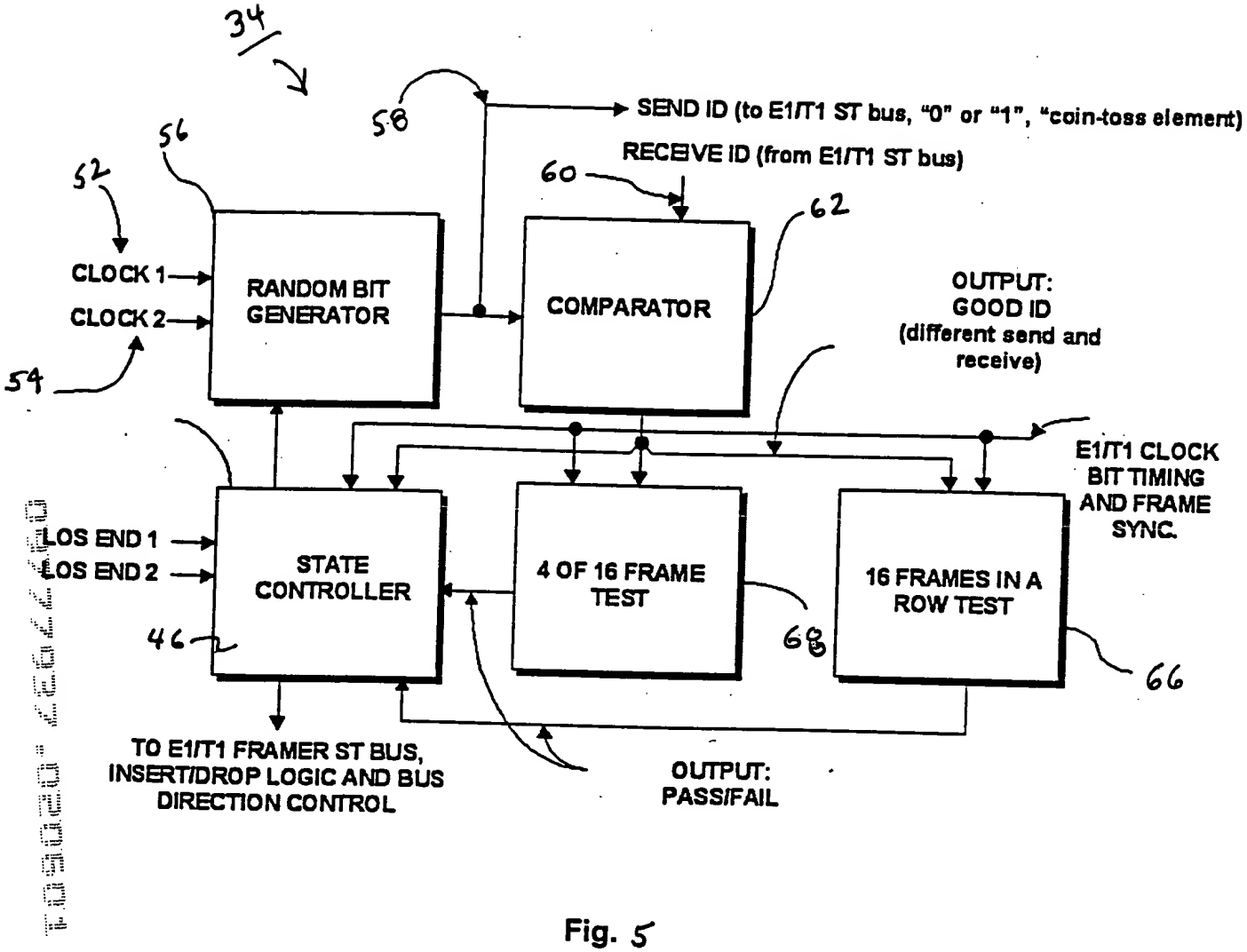

34
58
SEND ID (to E1/T1 ST bus, "0" or "1", "coin-toss element)
RECEIVE ID (from E1/T1 ST bus)
56
52
60
62
CLOCK 1
CLOCK 2
RANDOM BIT GENERATOR
COMPARATOR
OUTPUT: GOOD ID (different send and receive)
54
E1/T1 CLOCK BIT TIMING AND FRAME SYNC.
LOS END 1
LOS END 2
STATE CONTROLLER
4 OF 16 FRAME TEST
16 FRAMES IN A ROW TEST
46
68
66
TO E1/T1 FRAMER ST BUS, INSERT/DROP LOGIC AND BUS DIRECTION CONTROL
OUTPUT: PASS/FAIL

Fig. 5

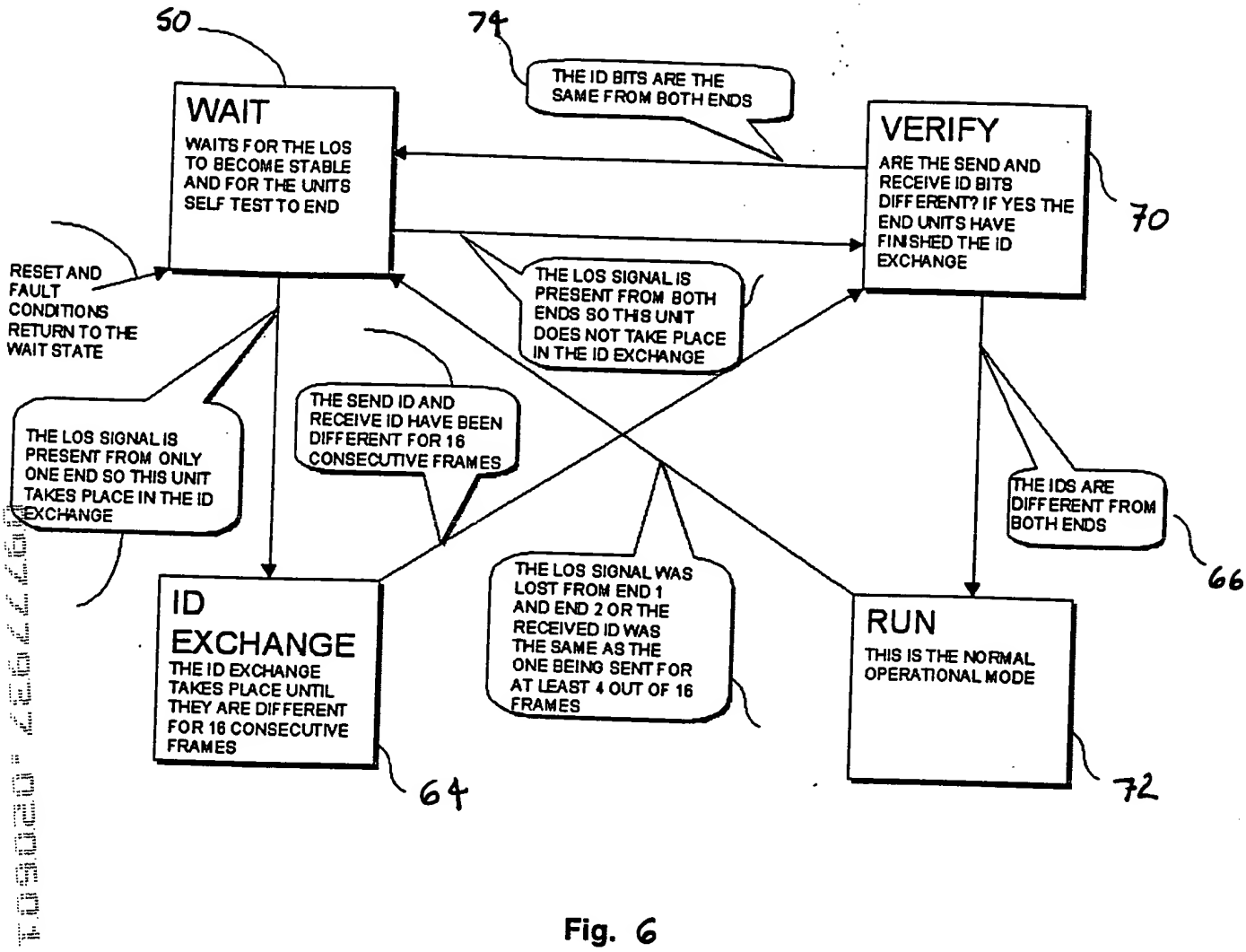

50
74
WAIT
WAITS FOR THE LOS TO BECOME STABLE AND FOR THE UNITS SELF TEST TO END
THE ID BITS ARE THE SAME FROM BOTH ENDS
VERIFY
ARE THE SEND AND RECEIVE ID BITS DIFFERENT? IF YES THE END UNITS HAVE FINISHED THE ID EXCHANGE
70
RESET AND FAULT CONDITIONS RETURN TO THE WAIT STATE
THE LOS SIGNAL IS PRESENT FROM BOTH ENDS SO THIS UNIT DOES NOT TAKE PLACE IN THE ID EXCHANGE
THE LOS SIGNAL IS PRESENT FROM ONLY ONE END SO THIS UNIT TAKES PLACE IN THE ID EXCHANGE
THE SEND ID AND RECEIVE ID HAVE BEEN DIFFERENT FOR 16 CONSECUTIVE FRAMES
THE IDS ARE DIFFERENT FROM BOTH ENDS
66
ID EXCHANGE
THE ID EXCHANGE TAKES PLACE UNTIL THEY ARE DIFFERENT FOR 16 CONSECUTIVE FRAMES
64
THE LOS SIGNAL WAS LOST FROM END 1 AND END 2 OR THE RECEIVED ID WAS THE SAME AS THE ONE BEING SENT FOR AT LEAST 4 OUT OF 16 FRAMES
RUN
THIS IS THE NORMAL OPERATIONAL MODE
72

Fig. 6

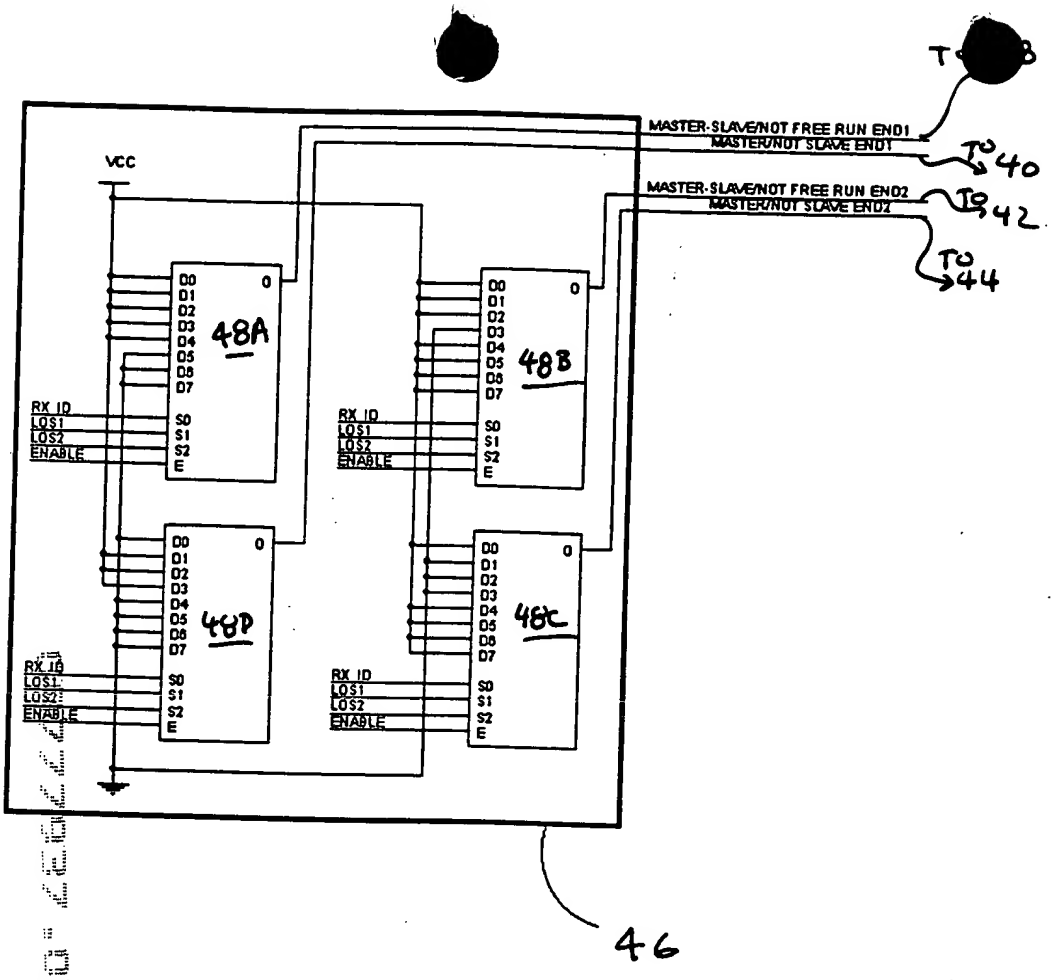

MASTER-SLAVE/NOT FREE RUN END1
MASTER/NOT SLAVE END1
MASTER-SLAVE/NOT FREE RUN END2
MASTER/NOT SLAVE END2
TO 40
TO 42
TO 44
VCC
48A
48B
48D
48C
D0
D1
D2
D3
D4
D5
D6
D7
O
RX ID
LOS1
LOS2
ENABLE
S0
S1
S2
E
46

Fig. 7

Fig 7A

Mode Table

LOS1	LOS2	Rx	Address	Master Slave	Free-run
0	0	0	0	end 2	end 1
0	0	1	1	end 1	end 2
0	1	0	2	end 1	end 2
0	1	1	3	end 1	end 2
1	0	0	4	end 2	end 1
1	0	1	5	end 2	end 1
1	1	0	6		
1	1	1	7		